PERFORMANCE ANALYSIS OF CURRENT MODE CARBON NANOTUBE ON-CHIP INTERCONNECT

A THESIS

Submitted by

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ABSTRACT

Recently, developments in VLSI technology improve the performance of integrated circuits (ICs) at an astonishing rate. The continuous growth in IC technology is made possible with the sustained scaling of transistors and interconnects. The semiconductor industry is facing a crucial problem in the interconnect section when IC is scaled down to 32nm technology node. Reduction in cross section of Copper interconnects increases its resistivity which results in excessive power dissipation, increasing signal latency and electromigration. Optical, Carbon Nanotube (CNT) and Graphene Nanoribbon (GNR) based interconnects are the promising candidates to solve the limitations in Copper interconnect. Optical interconnects offer low latency, high bandwidth and less power dissipation.

Optical interconnects are relatively larger in size and difficult to scale down its pitch below 0.6µm. CNT and GNR have more flexibility and less resistivity than Copper, thus, they can be implemented with the same scale or less than that of Copper interconnect. CNT is a graphene sheet rolled up to form a tube. According to the chirality vector, CNT exhibits metallic and semiconducting properties. Graphene Nanoribbon is constructed from unzipping of the Carbon Nanotubes. GNR shows metallic and semiconducting behaviour depending upon their termination style. The aim of this research work is to investigate and to enhance the performance of CNT interconnects for being as on-chip interconnects.

Initially, Single Walled CNT (SWCNT), Multi-Walled CNT (MWCNT) and SWCNT-bundle interconnects are designed and tested in voltage mode under 22nm technology in HSPICE. Their performances are analyzed and compared with Copper and optical interconnects. SWCNT-bundle and MWCNT interconnects overcome the high resistance problem in SWCNT with their parallel and concentric arrangement of CNTs. SWCNT-bundle and MWCNT exhibit analogous delay performance in local and semi-global interconnects. Whereas in global interconnect level, SWCNT-bundle performance is better as compared to MWCNT with 3Gbps bitrate and 0.9μW power dissipation. Optical interconnects offer less delay as compared with CNT structures in global but not in local. Next, in the comparison of the SWCNT-bundle performance with GNR, the overall performance of SWCNT-bundle is better than the GNR.

To improve the performance of SWCNT-bundle in the range of tera bits per sec (Tbps) and to reach comparable performance with optical interconnects, current signal transportation is introduced. In the current mode signaling, the interconnect line is terminated with short by current sensing circuit which avoids the charging of interconnect capacitance. This technique exploits the combined advantages of current mode signaling and SWCNT-bundle. Current mode signaling through SWCNT-bundle interconnect is simulated in MATLAB and HSPICE to study its efficiency and performance. The proposed current mode SWCNT–bundle is capable of transmitting the signal at the rate of 847Tbps in local and 38Gbps in global interconnect levels. It exhibits lesser delay and higher bitrate by the factor of 350 in local and 29 in global interconnect level as compared with voltage mode signaling. As compared to optical interconnects 1000 times lesser power delay product in local and 1.2 times in global with current mode SWCNT-bundle interconnects.

Carbon Nanotube Field Effect Transistor (CNTFET) based transceiver is proposed for on-chip SWCNT- bundle interconnect to ensure

the current mode signal through interconnect. Transceivers act as interfacing circuit between interconnects and devices present in ICs. In the proposed transceiver,. the transmitter architecture drives interconnect with lesser load, and the receiver section offers low impedance channel termination which results in speedy operation with low power dissipation. The proposed design utilizes the benefits of current mode signaling and unique characteristics of carbon nanotube. The designed CNTFET and MOSFET based transceivers are implemented with Stanford CNTFET model and TSMC BSIM4 model in HPSICE under 22nm technology. To test the performance of MOSFET and CNTFET based transceivers, Copper and metallic SWCNT-bundles are used as interconnects. The total interconnect link consists of transmitter, interconnect and receiver. CNTFET transmitters achieve 4 and 180 times lesser delay and 1.5 and 10^4 times lesser PDP as compared with MOSFET transcmitters in voltage mode and current mode signaling.

The Copper interconnect link with current mode exhibits 18 times lesser delay and 1.1 times more power dissipation as compared to voltage mode signaling. Whereas in SWCNT-bundle interconnect link, current mode shows lesser delay for signal propagation, and it dissipates lesser power by the factor of 27 and 225 while comparing with voltage mode, since the CNTFET transceiver design reduces the capacitive load in interconnects. The current mode SWCNT-bundle interconnect link with current mode transceiver is capable of trasmitting the signal up to 26Gbps in global interconnect level as expected by ITRS.

Finally, the performance of current mode SWCNT-bundle interconnect link is compared with optical interconnect link. It exhibits 1.8 times lesser delay and 10^4 orders lesser power delay product as compared to optical interconnect link. The MOSFET based transmitter and receiver circuits limit the performance of optical interconnect link whereas the current mode CNTFET transceiver shows outstanding performance in CNT interconnect link.

Among the all, current mode SWCNT-bundle interconnect with current mode CNTFET transceiver shows superior performance, and it can achieve high speed signal transmission with low power dissipation in future ICs. CNT can hold Moore's law for future technology nodes.